Hardware Design Job Interview Questions And Answers

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Hardware Design Interview Questions And Answers Guide.

Question - 1:

Explain what is Transmission Gate-based D-Latch?

Ans:

The Transmission-Gate input is connected to the D_LATCH data input (D), the control input to the Transmission-Gate is connected to the D_LATCH enable input (EN) and the Transmission-Gate output is the D_LATCH output (Q).

View All Answers

Question - 2:

How to detect sequence of "1101" arriving serially from signal line?

Ans:

Sequence detector : A sequence detector gives an output of 1 on detecting the given sequence else the output is zero.
Ex : if the given sequence to be detected is 111
and input stream is 1 1 0 1 1 1 0 0 1 0 1 1 1 1 1
the output should be 0 0 0 0 0 1 0 0 0 0 0 0 1 1 1.
Soln:
One of the different possible ways to detect a sequence is using a Mealy type FSM.
Using the following table the State machine can be designed.

View All Answers

Question - 3:

Which are the two ways of converting a two input NAND gate to an inverter?

Ans:

Short the two inputs of the nand gate and give the same input to the common wire,the nand gate works as an inverter.
One way is shorting the two inputs of the NAND gate and passing the input.
truth table:
A B output
1 1 0
0 0 1
The second way is passing the input to only one input(say A) of the NAND gate.Since the other input(say B) is floating, it is always logic one.
truth table:
A B output
1 1 0
0 1 1

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Question - 4:

How to design a divide-by-3 sequential circuit with 50% duty circle?

Ans:

take a counter with 3 f/f's that is to say with 6 states(2*3) now double the i/p clock frequency to the counter the o/p of the 3rd f/f is divide by 6 of the i/p with 50% duty cycle so effectively u got divide by 3 freq with 50% duty cycle.

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Question - 5:

Hardware Design interview questions part 5:

Ans:

41. What is equivalence checking?
42. What is the Moores law?
43. What is the difference between simulation and emulation?
44. What is the use of RTL?

45. State the differences between VHDL and Verilog?
46. What do you understand by synthesis?
47. Explain the bottom-up design process.
48. What are synchronous circuits?
49. How can distorted signals be identified with the use of SNR?
50. What are the various practices for improving SNR?

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Question - 6:

Hardware Design interview questions part 4:

Ans:

31. What are data flow diagrams?
32. What are compilers?
33. Explain the functioning of compilers.
34. What are microcontrollers?
35. Explain the functioning of microcontrollers.
36. What is assembly language?
37. What do you understand by interrupt latency?
38. Explain RTOS.
39. How does a binary counter works?
40. What are the numbers of bit combinations in a byte?

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Question - 7:

Hardware Design interview questions part 3:

Ans:

21. Give the truth table of a half-adder?
22. What are transmission gates?
23. What do you understand by DFT?
24. What are fault models?
25. Explain scan technologies
26. Explain BST?
27. What are the differences between BST and BIST?
28. State the differences between LFSR and MISR?
29. What is IDDQ?
30. What do you understand by the term recovery design?

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Question - 8:

Hardware Design interview questions part 2:

Ans:

11. What is the dissipation factor? How is it calculated?
12. Explain tolerance?
13. What is a potentiometer used for?
14. What are the various hardware design tools available?
15. What is a HDL?
16. How can a two input NAND gate be converted into an inverter?
17. Define set up time & hold time constraints?
18. Draw a circuit to divide the clock frequency by half.
19. Design a divide-by-3 sequential circuit with 50% duty circle.
20. What are adder circuits explain?

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Question - 9:

Hardware Design interview questions part 1:

Ans:

1. What are the various hardware design techniques?
2. What are passive components/
3. What are the various board design issues?
4. What are analog power supply systems?
5. What do you understand by overvoltage protection?
6. What is thermal management?
7. What is a breadboard?
8. What is the purpose of prototyping?
9. Explain the term dielectric absorption?
10. What do you understand by capacitor parasitic?

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Question - 10:

What are the different Adder circuits you studied?

Ans:

Adders are generally of five types:
1) Ripple Carry Adder:
The Ripple carry adder(RCA) consists of a building block named Half
Adder(HA) which is cascaded to form a Full Adder(FA). These building
blocks HAs and FAs are also the building blocks of all types of
adders.The n full adders are cascaded to form n bit RCA.
The full adder has three input pins(input Ai,input Bi,carryin Ci) and
two output pins(Sum and Ci+1).Its equations are:
Sum=Ai^Bi^Ci
Ci+1=Ai.Bi+Bi.Ci+Ai.Ci
2)Carry Lookahead Adder:
The Carry Lookahead Adder(CLA) reduces the delay as that in RCA. Let
Gi=Ai.Bi, and Pi=Ai^Bi, then Ci+1=Gi+Pi.Ci.
The expressions for Sum and Ci+1 is then defined completely in terms of
input pins rather wait for input carry to appear.
3)Carry Select Adder:
The carry select adder uses duplicate modules for each combination of
input carry(i.e. 1 and 0).The multiplexers then select the appropriate
sum and carry output according to the carry output of the preceding
stages.

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Question - 11:

What are set up time & hold time constraints? What do they signify? Which one is critical for estimating maximum clock frequency of a circuit?

Ans:

Suppose your flip-flop is positive edge triggered. time for which data should be stable prior to positive edge clock is called setup time constraint .
Time for which data should be stable after the positive edge of clock is called as hold time constraint.
if any of these constraints are violated then flip-flop will enter in meta stable state, in which we cannot determine the output of flip-flop.
there are two equation:
1. Tcq + Tcomb> Tskew + Thold
2. Tcq + Tcomb<Tskew +T - Tsetup
Tcq is time delay when data enters the flip-flop and data comes at output of flip flop.
Tcomb is the logic delay between two flip flop.
Tskew is the delay of clock to flip flop: suppose there are two flip flop ,if clock reaches first to source flip flop and then after some delay to destination flip flop ,it is
positive skew and if vice versa then negative skew.
so if you take 2 eq you will see that setup time is the determining factor of clock's time period.

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Question - 12:

Give a circuit to divide frequency of clock cycle by two?

Ans:

You can divide the frequency of a clock by just implementing T Flip flop.
Give clock as clock input and tie the T input to logic 1.

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Question - 13:

How do you detect if two 8-bit signals are same?

Ans:

XOR each bits of A with B (for eg A[0] xor B[0]) and
so on. the o/p of 8 xor gates are then given as i/p to
an 8-i/p nor gate. if o/p is 1 then A=B.

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Question - 14:

Give two ways of converting a two input NAND gate to an inverter.

Ans:

One way is shorting the two inputs of the NAND gate and passing the input.
truth table:
A B output
1 1 0
0 0 1
The second way is passing the input to only one input(say A) of the NAND gate.Since the other input(say B) is floating, it is always logic one.
truth table:
A B output
1 1 0
0 1 1

View All Answers

Question - 15:

Design a divide-by-3 sequential circuit with 50% duty circle.

Ans:

Take a smiths counter with 3 f/f's
that is to say with 6 states(2*3)
now double the i/p clock frequency to the counter
the o/p of the 3rd f/f is divide by 6 of the i/p with 50% duty cycle
so effectively u got divide by 3 freq with 50% duty cycle

Question - 16:

Give the truth table for a Half Adder. Give a gate level implementation of the same.

Ans:

TRUTH TABLE FOR HALF ADDER:
A B SUM CARRY
0 0 0 0
0 1 1 0
1 0 1 0
1 1 0 1
IMPLEMENTATION:
For SUM, The two inputs A and B are given to XOR gate.
For Carry, The two inputs A and B are given to AND gate.

Question - 17:

How do you detect a sequence of "1101" arriving serially from a signal line?

Ans:

Sequence detector : A sequence detector gives an output of 1 on detecting the given sequence else the output is zero.
Ex : if the given sequence to be detected is 111
and input stream is 1 1 0 1 1 1 0 0 1 0 1 1 1 1 1
the output should be 0 0 0 0 0 1 0 0 0 0 0 0 1 1 1.
Soln:
One of the different possible ways to detect a sequence is using a Mealy type FSM.
Using the following table the State machine can be designed.
since the number of bits in the sequence 1101 is 4 we have 4 states

```
---------------------------------------------------
|PS | Seq detected by the state | NS/output |
| | |--------------|
| | | | X=0 | X=1 |
|---------------------------------------------------
| S1 | - | S1/0 | S2/0 |
|---------------------------------------------------|
| S2 | 1 | S1/0 | S3/0 |
|---------------------------------------------------|
| S3 | 11 | S4/0 | S3/0 |
|---------------------------------------------------|
| S4 | 110 | S1/0 | S2/1 |
|---------------------------------------------------|
```
when in state S4 (PS),and input(X) from the sequence is 1,the sequence "1101" has been detected once and (to find the next state select the longest "seq identified by a state" column that matches part of the sequence 1101--ie.,1 or 01 or 101 ....)the NS is S2 since the sequence detected by the state S2 is 1(in 1101- 01 or 101 ,etc are not present in the seq identified by the state column ,)

Question - 18:

Suppose you have a combinational circuit between two registers driven by a clock. What will you do if the delay of the combinational circuit is greater than your clock signal?

Ans:

Use the concept of register-retiming.
divide the total combinatorial delay in two segments such that individually the delay is less the clock period.
this can be done by inserting a flip-flop in the combinational path.
e.g,
clock period --- 5 ns
total cominational delay ---- 7
then divide the 7ns path in two path of 4 or 3 (best results are obtained if delays are same for both path i.e 3.5ns) by inserting a flip-flop in between.

Question - 19:

Draw a Transmission Gate-based D-Latch?

Ans:

The Transmission-Gate's input is connected to the D_LATCH data input (D), the control input to the Transmission-Gate is connected to the D_LATCH enable input (EN) and the Transmission-Gate output is the D_LATCH output (Q)

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