Computer Architecture Job Interview Questions And Answers

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Computer Architecture Interview Questions And Answers Guide.

Question - 1:

Convert a number to its two?s compliment and back?

Ans:

ay for example 5 is a decimal no converts it into binary format is 0101 base 2 invert this binary value 1010 add 1 with this ans we will get 2's complement of this given no is 1011

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Question - 2:

Explain What is MESI?

Ans:

MESI stands for a protocol which is followed in shared processor systems. M - Modified E - Exclusive S - Shared I - Invalid

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Question - 3:

What are the components in a Microprocessor?

Ans:

its a general purpose register. its components are one processor along with external ROM, RAM, etc
MICROPROCESSOR IS A PROCESSOR(CPU) embedded in a single chip BY VLSI DESIGN. RATHER,IT IS A CLOCK-DRIVEN,PROGRAM CONTROLLED CHIP

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Question - 4:

What is ACBF(Hex) divided by 16?

Ans:

6 5 0110 0101

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Question - 5:

Convert 65(Hex) to Binary?

Ans:

10000000 1's complement of it is 01111111 +1 ---------- 1000000

View All Answers

Question - 6:

For a pipeline with n stages, what is the ideal throughput? What prevents us from achieving this ideal throughput?

Ans:

With "n" stage pipeline the throughput should be "n" instructions.
As the pipe stages can't be perfectly balanced (time to perform task in a pipeline stage), furthermore pipeline does involve some overheads.

View All Answers

Question - 7:

Explain What are the five stages in a DLX pipeline?

Ans:

The instruction sets can be differentiated by
* Operand storage in the CPU
* Number of explicit operands per instruction
* Operand location
* Operations
* Type and size of operands
Submitted by Sowjanya Rao (Sowjanya_Rao@Dell.com)
IF: Instruction Fetch (from memory) ID: Instruction decode and register read EX: Execution of the operation or address calculation MEM: Data memory access (i.e accessing the operand) WB: Write Back (the result)

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Question - 8:

Explain What are the different hazards? How do you avoid them?

Ans:

There are situations, called hazards, that prevent the next instruction in the instruction stream from executing during its designated clock cycle. Hazards reduce the performance from the ideal speedup gained by pipelining. There are three classes of Hazards:
1. Structural Hazards: It arise from resource conflicts when the hardware cannot support all possible combinations of instructions simultaniously in ovelapped execution.
2. Data Hazards: It arise when an instruction depends on the results of previous instruction in a way that is exposed by the ovelapping of instructions in the pipeline.
3. Control Hazards: It arise from the pipelining of branches and other instructions that change the PC.
How to Avoid Hazards:
1. Structural Hazard: This arise when some functional unit is not fully pipelined. Then the sequence of instructions using that unpipelined unit cannot proceed at the rate of one one per clock cycle. Another common way that it may appear is when some resources are not duplicated enough to allow all combination of instructionsin the pipeline to execute. So by fully pipelining the stages and duplicating resouces will avoid structural pipeline.
2. Data Hazards: A major effect of pipelining is to change the relative timing of instructions by overlapping their execution. This overlap introduce the data and control hazards. Data hazards occur when the pipeline changes the order of read/write accesses to operands so that the order differs from the order seen by sequentially executing instructions on an unpipelined processor. It can be mimimized by simple hardware technique called forwarding or by adding stalls.
3. Control Hazards: They are also know as Branch Hazards. The simplest scheme to handle branches hazard is to freeze or flush the pipeline, holding or deleting any instructions after the branch until the branch destination is known. In this case branch penalty is fixed and cannot be reduced by software. The other scheme is predicted-not-taken or predicted-untaken and delayed branch.

View All Answers

Question - 9:

What are Branch Prediction and Branch Target Buffers?

Ans:

By vectoring technique.

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Question - 10:

Explain What is a cache?

Ans:

It turns out that caching is an important computer-science process that appears on every computer in a variety of forms. There are memory caches, hardware and software disk caches, page caches and more. Virtual memory is even a form of caching.
Caching is a technology based on the memory subsystem of your computer. The main purpose of a cache is to accelerate your computer while keeping the price of the computer low. Caching allows you to do your computer tasks more rapidly. Cache technology is the use of a faster but smaller memory type to accelerate a slower but larger memory type. A cache has some maximum size that is much smaller than the larger storage area. It is possible to have multiple layers of cache.
A computer is a machine in which we measure time in very small increments. When the microprocessor accesses the main memory (RAM), it does it in about 60 nanoseconds (60 billionths of a second). That's pretty fast, but it is much slower than the typical microprocessor. Microprocessors can have cycle times as short as 2 nanoseconds, so to a microprocessor 60 nanoseconds seems like an eternity.
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What if we build a special memory bank in the motherboard, small but very fast (around 30 nanoseconds)? That's already two times faster than the main memory access. That's called a level 2 cache or an L2 cache. What if we build an even smaller but faster memory system directly into the microprocessor's chip? That way, this memory will be accessed at the speed of the microprocessor and not the speed of the memory bus. That's an L1 cache, which on a 233-megahertz (MHz) Pentium is 3.5 times faster than the L2 cache, which is two times faster than the access to main memory.
Some microprocessors have two levels of cache built right into the chip. In this case, the motherboard cache -- the cache that exists between the microprocessor and main system memory -- becomes level 3, or L3 cache.

View All Answers

Question - 11:

What is the difference between Write-Through and Write-Back Caches? Explain advantages and disadvantages of each?

Ans:

Writing in cache is possible through two method. 1. Write back-update the cache memory along with main memory. 2. Write through-writing in cache only, equivalent copy is produce in main memory, when word is not updated from a long time.
Writing in cache is possible through two method. 1. Write back-update the cache memory along with main memory. 2. Write through-writing in cache only, equivalent copy is produce in main memory, when word is not updated from a long time.

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Question - 12:

Cache Size is 64KB, Block size is 32B and the cache is Two-Way Set Associative. For a 32-bit physical address, give the division between Block Offset, Index and

Tag.

Ans:

if block size is 32B,then block offset = 2^5 so 5 bits, index has equation, cache size/(block size*associative) so 64K/(32*2) = 1K, 2^10, so index = 10 bits,now tag = physical address-block offset-index, which is 32-5-10 = 17bits

View All Answers

Question - 13:

Explain What is Virtual Memory?

Ans:

Virtual memory is a concept that, when implemented by a computer and its operating system, allows programmers to use a very large range of memory or storage addresses for stored data. The computing system maps the programmer's virtual addresses to real hardware storage addresses. Usually, the programmer is freed from having to be concerned about the availability of data storage.
In addition to managing the mapping of virtual storage addresses to real storage addresses, a computer implementing virtual memory or storage also manages storage swapping between active storage (RAM) and hard disk or other high volume storage devices. Data is read in units called "pages" of sizes ranging from a thousand bytes (actually 1,024 decimal bytes) up to several megabyes in size. This reduces the amount of physical storage access that is required and speeds up overall system performance.

View All Answers

Question - 14:

Whats the difference between Write-Through and Write-Back Caches? Explain advantages and disadvantages of each?

Ans:

The comparison can be made out of two factors
1) Performance and
2) Integrity of Data
Write through is better in integrity as it will flush for each writes.
Write back holds up the write till the same cache line has to be used up for a read, which question the data integrity when multiple processors access the same region of data using its own internal cache.
Write Back - gives a good performance, as it save many memory write cycles /write.
Write Through - Doesn't give this performance compared to the write-back.

View All Answers

Question - 15:

How do you handle precise exceptions or interrupts?

Ans:

Like java have a feature for handling exception handling "prime catch".the exception like divide by zero,out of bound.

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Question - 16:

For a pipeline with "n" stages, whats the ideal throughput? What prevents us from achieving this ideal throughput?

Ans:

With "n" stage pipeline the throughput should be "n" instructions.
As the pipe stages can't be perfectly balanced (time to perform task in a pipeline stage), furthermore pipeline does involve some overheads.

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Question - 17:

What is the difference between interrupt service routine and subroutine?

Ans:

Subroutine are the part of executing processes(like any process can call a subroutine for achieve task),while the interrupt subroutine never be the part.interrupt subroutine are subroutine that are external to a process.

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Question - 18:

The CPU is busy but you want to stop and do some other task. How do you do it?

Ans:

Arise a non maskable interrupt.
Then give jump instruction to required subroutine.

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Question - 19:

Convert a number to its twos compliment and back?

Ans:

First convert a number into binary format. Then keep last binary number as it is & complement all others.
Eg:- 1101001
2's Compl:0010111

View All Answers

Question - 20:

Convert 65(Hex) to Binary?

Ans:

65 to decimal
65/16=4
remainder=1
==41 decimal
decimal to binary
101001

View All Answers

Question - 21:

What is a cache?

Ans:

It turns out that caching is an important computer-science process that appears on every computer in a variety of forms. There are memory caches, hardware and software disk caches, page caches and more. Virtual memory is even a form of caching.
Caching is a technology based on the memory subsystem of your computer. The main purpose of a cache is to accelerate your computer while keeping the price of the computer low. Caching allows you to do your computer tasks more rapidly. Cache technology is the use of a faster but smaller memory type to accelerate a slower but larger memory type. A cache has some maximum size that is much smaller than the larger storage area. It is possible to have multiple layers of cache.
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Question - 22:

What are the five stages in a DLX pipeline?

Ans:

The instruction sets can be differentiated by
* Operand storage in the CPU
* Number of explicit operands per instruction
* Operand location
* Operations
* Type and size of operands

View All Answers

Question - 23:

What is Virtual Memory?

Ans:

Virtual Memory is a way of extending a computers memory by using a disk file to simulate add'l memory space. The OS keeps track of these add'l memory addresses on the hard disk called pages, and the operation in bringing in pages is called page fault.

View All Answers

Question - 24:

What is Cache Coherency?

Ans:

Cache coherence refers to the integrity of data stored in local caches of a shared resource. Cache coherence is a special case of memory coherence. When clients in a system, particularly CPUs in a multiprocessing system cache occurs.

View All Answers

Question - 25:

What is a Snooping cache?

Ans:

DNS cache snooping is not a term the author just made up, it is known and discussed by some notable
DNS implementation developers, and a few interested DNS administrators have probably at least heard of it.

View All Answers

Question - 26:

Cache Size is 64KB, Block size is 32B and the cache is Two-Way Set Associative. For a 32-bit physical address, give the division between Block Offset, Index and Tag.

Ans:

64k/32 = 2000 blocks
2 way set assoc- 2000/2 = 1000 lines-> 10 bits for index
32B block-> 5 bits for block offset
32-10-5= 17 bits for tag

View All Answers

Question - 27:

What is the pipelining?

Ans:

A technique used in advanced microprocessors where the microprocessor begins executing a second instruction before the first has been completed. That is, several instructions are in the pipeline simultaneously, each at a different processing stage.

View All Answers

Question - 28:

What are the different hazards? How do you avoid them?

Ans:

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Question - 29:

What is MESI?

Ans:

The MESI protocol is also known as Illinois protocol due to its development at the University of Illinois at Urbana-Champaign and MESI is a widely used cache coherency and memory coherence protocol.
MESI is the most common protocol which supports write-back cache. Its use in personal computers became widespread with the introduction of Intel's Pentium processor to "support the more efficient write-back cache in addition to the write-through cache previously used by the Intel 486 processor"

View All Answers

Question - 30:

What are the basic components in a Microprocessor?

Ans:

1)address lines to refer to the address of a block
2)data lines for data transfer
3)IC chips 4 processing data

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